Tri (X,Y,Z) Axis Accelerometer Specifications

PART NUMBER:

KXM52-1050

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	APPROVED BY	DATE
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MEMS MGR.	Scott Miller	4/25/06
ASIC MGR.	Jim Groves	7/12/05
VP ENG.	Tim Davis	7/12/05
VP SALES	Bruce Finke	7/12/05

ECN #	REV	PG #	REVISION DESCRIPTION	DATE	REV'D BY
05-027	1	5	Added Test Specification	7/12/05	Scott Miller
06-004	2		Updated specification to new format	3/23/06	A. Bergstrom, S. Miller

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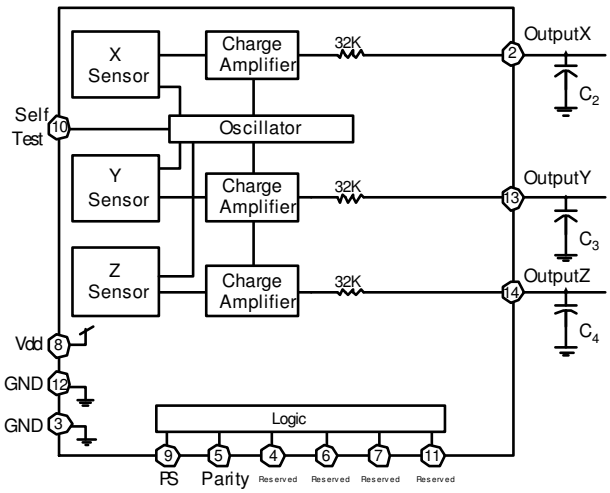
Product Description

The KXM52-1050 is a three axis, analog output silicon micromachined accelerometer with a full-scale output range of ±2.0g (19.6 m/s^2). Plasma micromachining is used to fabricate the sense element using Kionix's proprietary deep reactive ion etch processes. Kionix linear accelerometers function on the principle of differential capacitance; acceleration causes displacement of a silicon structure resulting in a capacitance change. Common mode cancellation is used to decrease errors from process variation, temperature, and environmental stress. The sense element is hermetically sealed at the wafer level by bonding a silicon lid wafer to the device using glass frit. A separate ASIC device packaged with the sense element provides signal conditioning and self-test. The accelerometer is delivered in a 5 x 5 x 1.8 mm Dual Flat No-lead (DFN) package.

Functional Diagram



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Product Specifications

Table 1. Mechanical

(specifications are for operation at V_{dd} = 3.3V and T = 25ºC unless stated otherwise)

Parameters	Units	Min	Target	Max
Operating Temperature Range	ºC	-40	-	85
Zero-g Offset	V	1.617	1.650	1.683
Zero-g Offset Variation from RT over Temp.	mg	-150	-	150
Sensitivity	mV/g	653	660	667
Sensitivity Variation from RT over Temp.	%	-2	0	+2
Offset Ratiometric Error (V_{dd} = 3.3V ± 5%)	%	-	0.4	1.5
Sensitivity Ratiometric Error (V_{dd} = 3.3V ± 5%)	%	-	0.4	1.5
Non-Linearity	% of FS	-	0.1	0.5
Cross Axis Sensitivity	%	-	2.0	3.0
Self Test Output change on Activation	g	1.0 (xy) 0.2 (z)	1.1 (xy) 0.4 (z)	1.2 (xy) 0.6 (z)
Bandwidth (-3dB)[1]	Hz	-	-	3100 (XY) 1300 (Z)
Noise Density (on filter pins)	µg / √Hz	-	35 (xy) 65 (z)	100

Notes:

1. User definable with external capacitors. Maximum defined by the frequency response of the sensors.

Table 2. Electrical

(specifications are for operation at V_{dd} = 3.3V and T = 25ºC unless stated otherwise)

Parameters		Units	Min	Target	Max
Supply Voltage (V_{dd})	Operating	V	2.5	3.3	5.5
Current Consumption	Operating[1]	mA	1.3	1.7	2.3
	Standby	µA	-	-	10
Analog Output Resistance(R_{out})		kΩ	24	32	40
Power Up Time[1]		ms		5*R_{out}*C	

Notes:

1. Power up time is determined by 5 times the RC time constant of the user defined low pass filter.

Table 3. Environmental

Parameters		Units	Min	Target	Max
Supply Voltage (V_{dd})	Absolute Limits	V	-0.3	-	7.0
Operating Temperature Range		ºC	-40	-	85
Storage Temperature Range		ºC	-55	-	150
Mech. Shock (powered and unpowered)		g	-	-	4600 for 0.5ms
ESD	HBM	V	-	-	3000

Caution: ESD Sensitive and Mechanical Shock Sensitive Component, improper handling can cause permanent damage to the device.

The 14-pin DFN package conforms to European Union Directive 2002/95/EC on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS).

Application Schematic and Pin Function Table

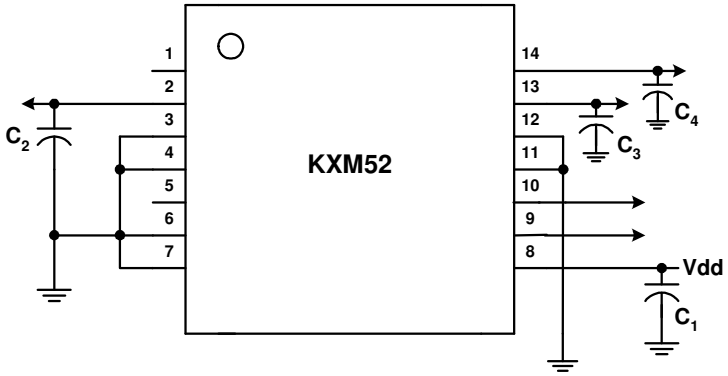

Table 4. KXM52 Pin Descriptions

Pin	Name	Description
1	NC	Not Connected Internally.
2	X Output	Analog output of the x-channel. Optionally, a capacitor (C_2) placed between this pin and ground will form a low pass filter.
3	GND	Ground
4	Reserved	Factory reserved. Connect this pin to ground.
5	Parity	Checks EEPROM for parity error.
6	Reserved	Factory reserved. Connect this pin to ground.
7	Reserved	Factory reserved. Connect this pin to ground.
8	Vdd	The power supply input. Decouple this pin to ground with a 0.1uF ceramic capacitor (C_1).
9	PS	When the PS pin is connected to GND or left floating, the KXM52 is shutdown and drawing very little power. When the PS pin is tied to Vdd, the unit is fully functional.
10	ST	Self Test. Output X, Output Y, and Output Z of a properly functioning part will increase when Vdd is applied to the self test pin.
11	Reserved	Factory reserved. Connect this pin to ground.
12	GND	Ground
13	Y Output	Analog output of y-channel. Optionally, a capacitor (C_3) placed between this pin and ground will form a low pass filter.
14	Z Output	Analog output of z-channel. Optionally, a capacitor (C_4)placed between this pin and ground will form a low pass filter.

Application Design Equations

The bandwidth is determined by the filter capacitors connected from pins 2, 13 and 14 to ground. The response is single pole. Given a desired bandwidth, f_{BW}, the filter capacitors are determined by:

$$C_2 = C_3 = C_4 = \frac{4.97x10^{-6}}{f_{BW}}$$

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Test Specifications

***Special Characteristics**:*

These characteristics have been identified as being critical to the customer. Every part is tested to verify its conformance to specification prior to shipment.

Parameters		Specification	Test Conditions
Zero-g Offset @ RT		1.650 ± 0.033 V	25ºC, V_{dd} = 3.3V
Sensitivity @ RT		660 ± 7 mV/g	25ºC, V_{dd} = 3.3V
Cross Axis Sensitivity		< 3%	25ºC, V_{dd} = 3.3V
Current Consumption	Operating	1.3 <= I_{dd} <= 2.0 mA	25ºC, V_{dd} = 3.3V

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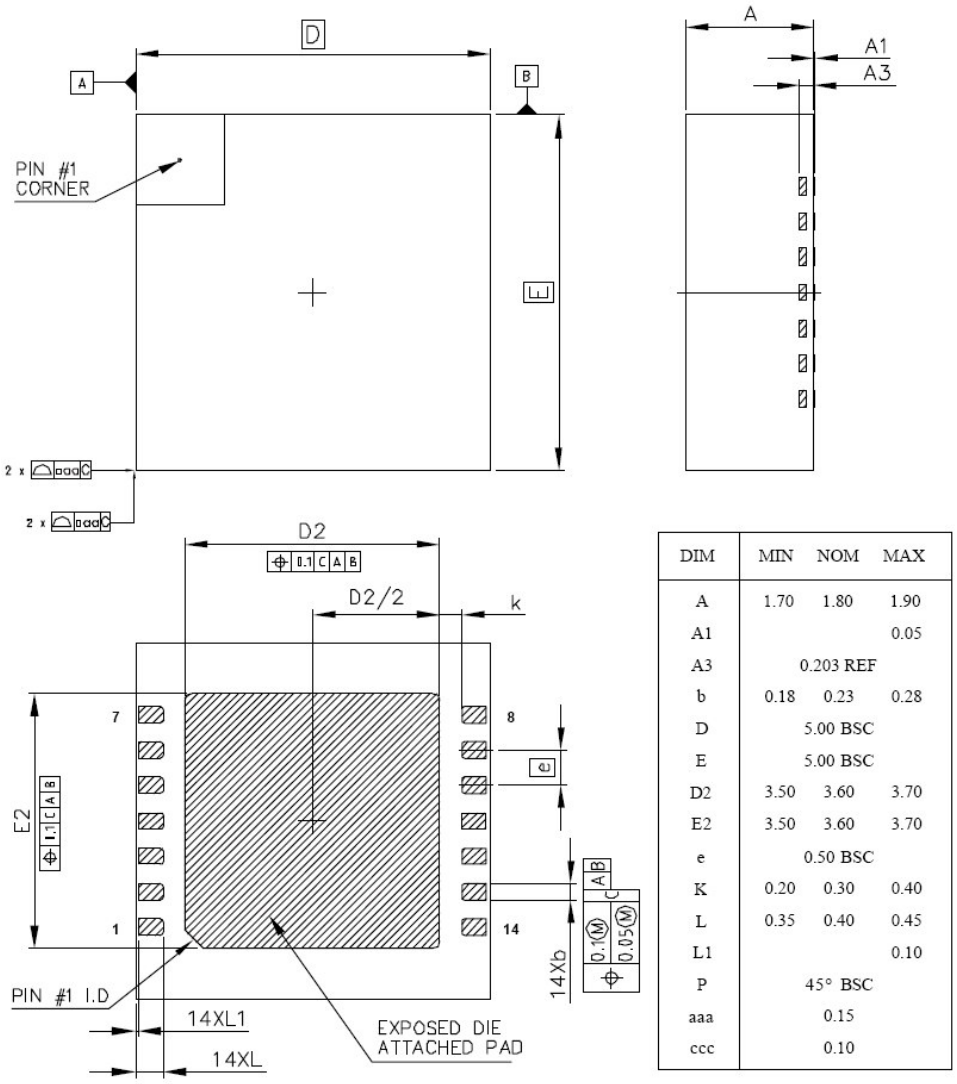
Package Dimensions



DIM	MIN	NOM	MAX
A	1.70	1.80	1.90
A1			0.05
A3		0.203 REF	
b	0.18	0.23	0.28
D		5.00 BSC	
E		5.00 BSC	
D2	3.50	3.60	3.70
E2	3.50	3.60	3.70
e		0.50 BSC	
K	0.20	0.30	0.40
L	0.35	0.40	0.45
L1			0.10
P		45° BSC	
aaa		0.15	
ccc		0.10	

NOTES

1.0 DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.

2.0 ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

3.0 DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP. DIMENSION L1 REPRESENTS TERMINAL FULL BACK FROM PACKAGE EDGE UP TO 0.1mm IS ACCEPTABLE.

4.0 COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.

5.0 RADIUS ON TERMINAL IS OPTIONAL.

Package Orientation