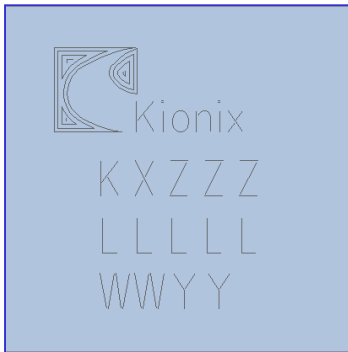


This technical note is intended to provide information about Kionix's 5 x 5 mm DFN packages and guidelines for developing PCB land pattern layouts. These guidelines are general in nature and based on recommended industry practices. The user must apply their actual experiences and development efforts to optimize designs and processes for their manufacturing techniques and the needs of varying end-use applications. It should be noted that with the proper PCB footprint and solder stencil designs, the package will self-align during the solder reflow process.

DFN Package Marking



- Marking font type : Arial
 - Font size : 1.5 Point (0.56 mm height)
 - Line space : 0.3 mm
 - Text information :
 - 1st line – Logo (No additional dot type pin#1 mark)
 - 2nd line – Device name
 - 3rd line – Assembly Build Lot code
 - 4th line – Date code (WWYY)
- Note - 2nd ~ 4th line text shall be left justified.

Figure 1. DFN package marking information.

DFN Package Outline and Dimensions

As a starting point, the following diagrams show the outline of the 5 x 5 DFN packages with dimensions and tolerances. All dimensions and tolerances conform to ASME Y14.5M-1994. All dimensions are in millimeters and angles are in degrees.

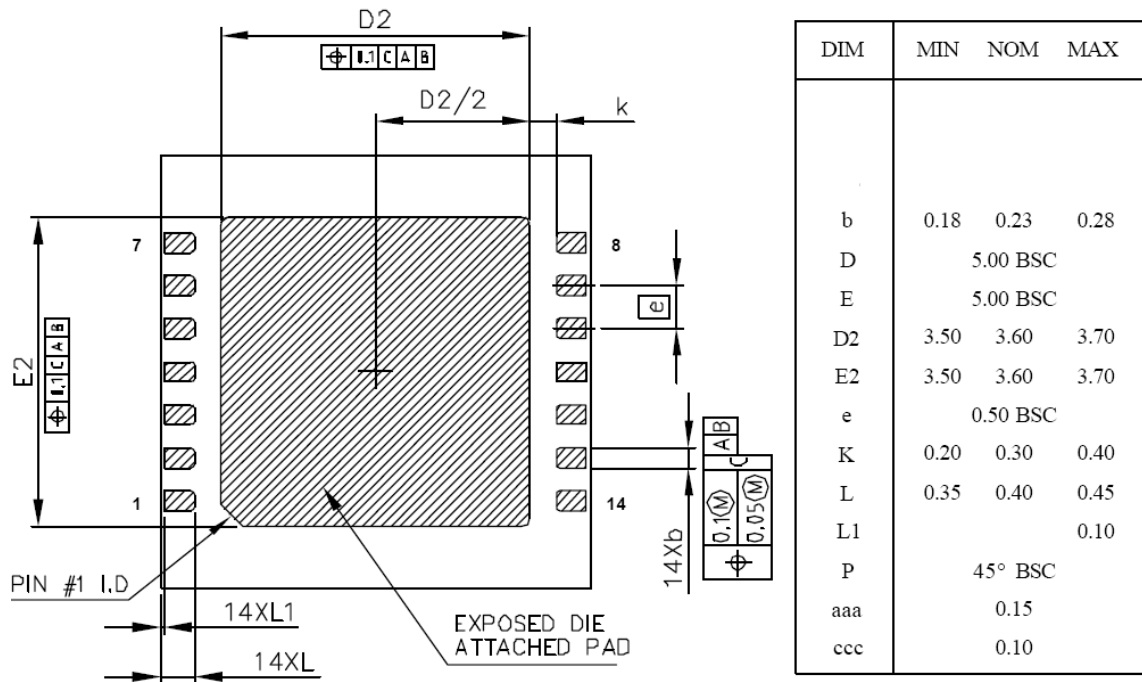


Figure 2. 5 x 5 x 1.8 mm package outline diagram with dimensions.

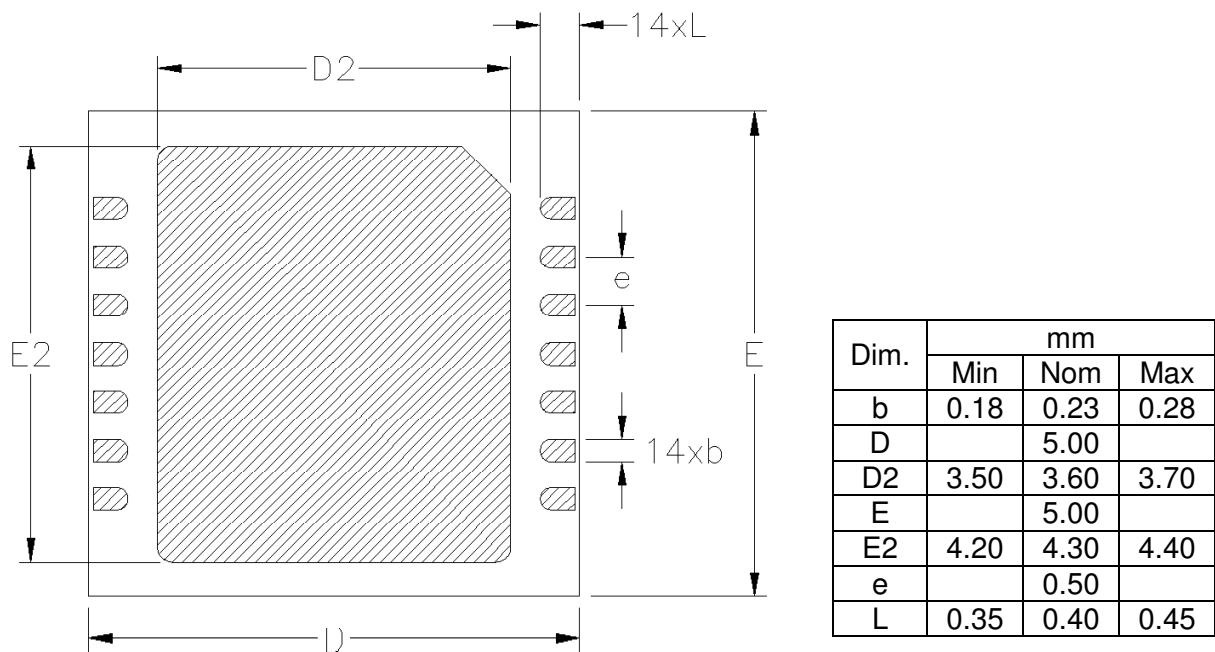


Figure 3. 5 x 5 x 1.2 mm package outline diagram with dimensions.

DFN PCB Layout Recommendations

Given the above package dimensions, the following guidelines are recommended:

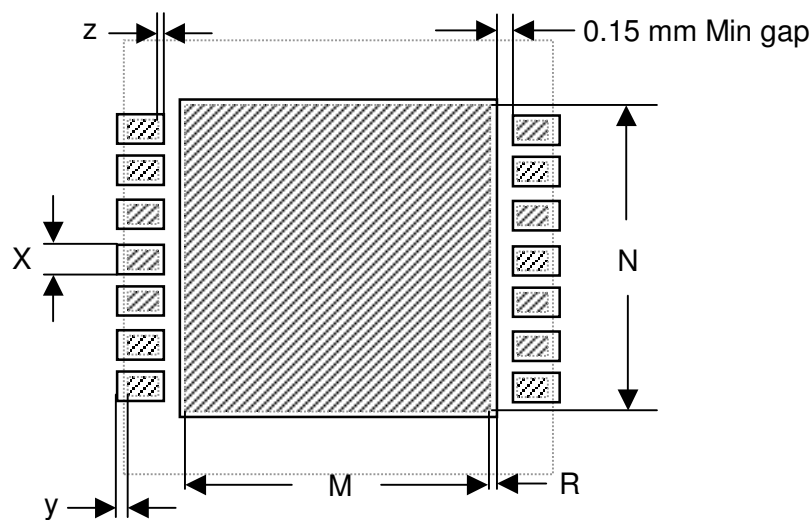


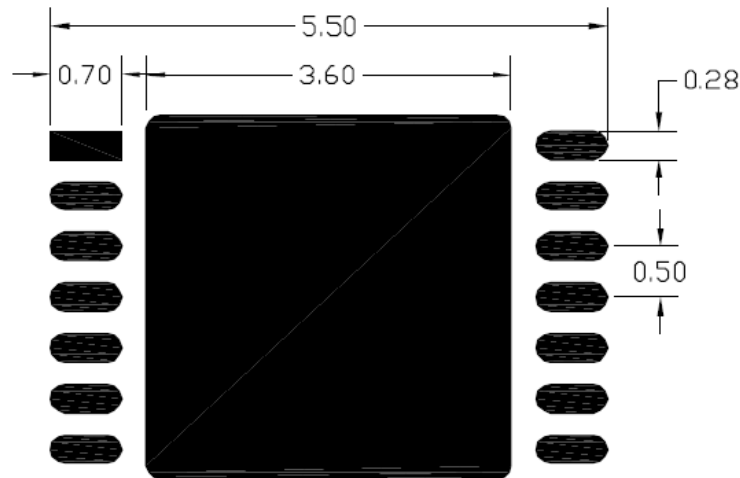
Figure 4. Land pattern layout with package overlay

Nominal Package I/O Pad Dimensions (mm)			I/O Land Dimension Guidelines (mm)		
Pad Pitch (e)	Pad Width (b)	Pad Length (L)	Land Width (X)	Outward Extension (y)	Inward Extension (z)
0.5	0.23	0.4	0.28 Nom	0.15 Min	0.05 Min

The perimeter I/O lands are slightly larger on all sides than the package I/O pads. The outward extension (y) of the I/O lands can be increased beyond the 0.15 mm minimum, when PCB area is available. However, any increase in the inward extension (z) must consider the effect on the isolation gap to the center pad. This gap must not be less than 0.15 mm to avoid shorting.

Nominal Package Center Pad Dimensions (mm)			Center Pad Land Dimension Guidelines (mm)		
	Pad Width (D2)	Pad Length (E2)	Land Width (M)	Land Length (N)	Outward Extension (R)
5 x 5 x 1.8	3.6	3.6	3.6	3.6	0 - 0.15 Max
5 x 5 x 1.2	3.6	4.3	3.6	4.3	0 - 0.15 Max

The center pad land should be designed 0 mm to 0.15 mm larger per side than the package's exposed center pad. An example of a PCB land pad layout is shown in Figure 5.



PCB PAD LAYOUT

Figure 5. Example of a PCB land pad layout for the 5 x 5 x 1.8 mm DFN package.

DFN Solder Stencil Guidelines

A laser-cut, stainless steel stencil with electro-polished trapezoidal walls is recommended.

Solder stencil thickness: 0.125mm

Re-flowed solder joints on the PCB perimeter I/O lands should have about a 50 to 75 μm (2 to 3 mil) standoff height. To achieve this, the stencil aperture size-to-land size should typically be a 1:1 ratio.

To reduce solder paste volume on the center pad, it is recommended that an array of smaller apertures be used instead of one large aperture. The smaller apertures can be circular or square and of various dimensions and array sizes. The main goal should be a dimensional combination that results in a 40% - 80% solder paste coverage. This reduced coverage on the center pad is important in achieving good coverage without excessive standoff or bridging to the PCB perimeter I/O lands. An example layout is given in the following figure:

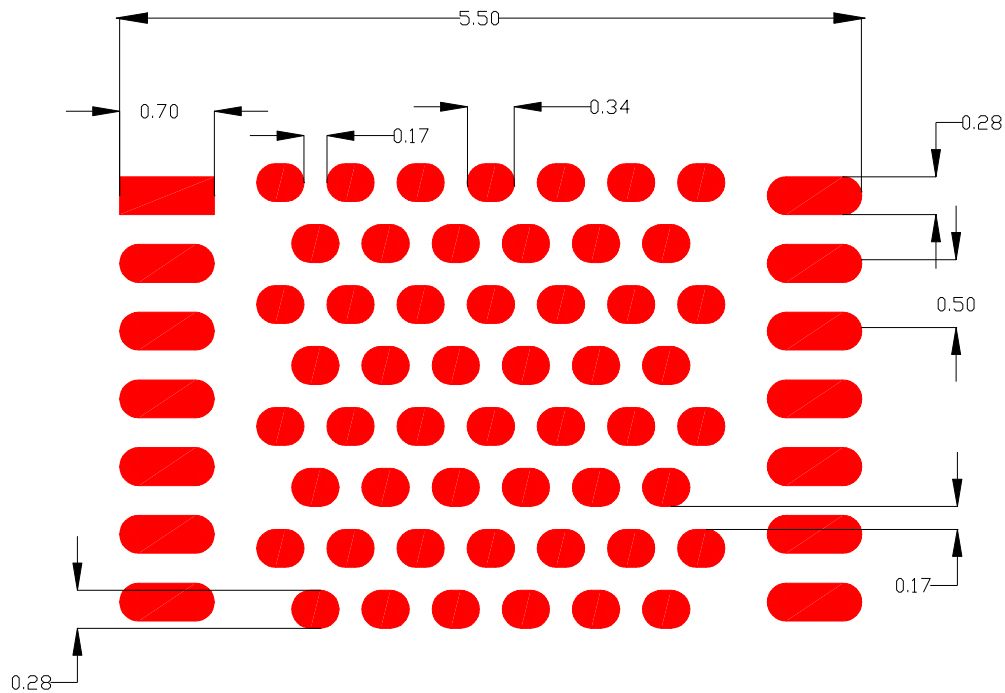


Figure 6. Example of a 5 x 5 x 1.8 mm DFN solder stencil layout.

Traces, Vias

Vias are not needed for thermal dissipation, as our part doesn't generate much heat. Therefore, only electrical vias are needed. If vias are not in the land pads, capped, plugged, tented, un-capped or un-plugged vias can be used. To ensure optimal performance, vias and traces should not be placed on the top layer directly beneath the accelerometer. The following figures illustrate an example of proper PCB via and trace placement. Obviously, each product will present its own physical limitations for accelerometer placement and trace routing. Therefore, these guidelines are general in nature. Engineering judgment should be used to try to avoid placement directly beneath the accelerometer.

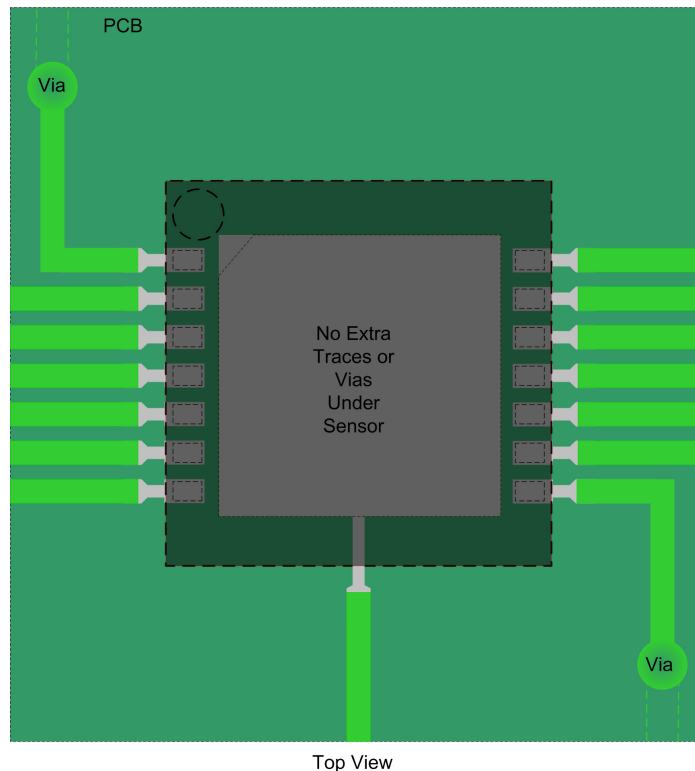


Figure 7. Via and Trace “Keepout” (Top View)

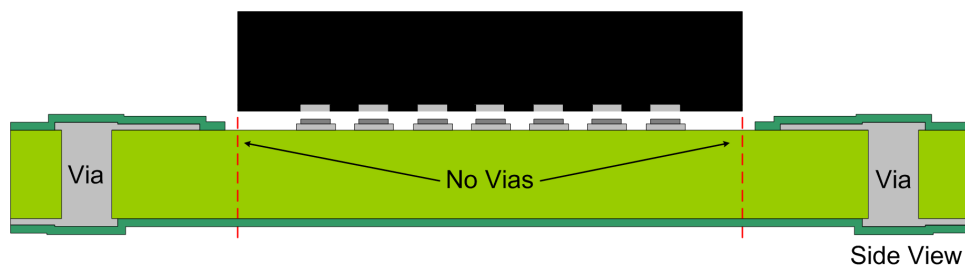


Figure 8. Via and Trace “Keepout” (Side View)

Tape and Reel Dimensions

The following section provides information on the tape and reel used for shipping Kionix's 5 x 5 mm DFN accelerometers.

Package	Tape Width	Component Pitch	Hole Pitch	Reel Diameter
DFN (5x5)	16mm	8mm	4mm	330mm

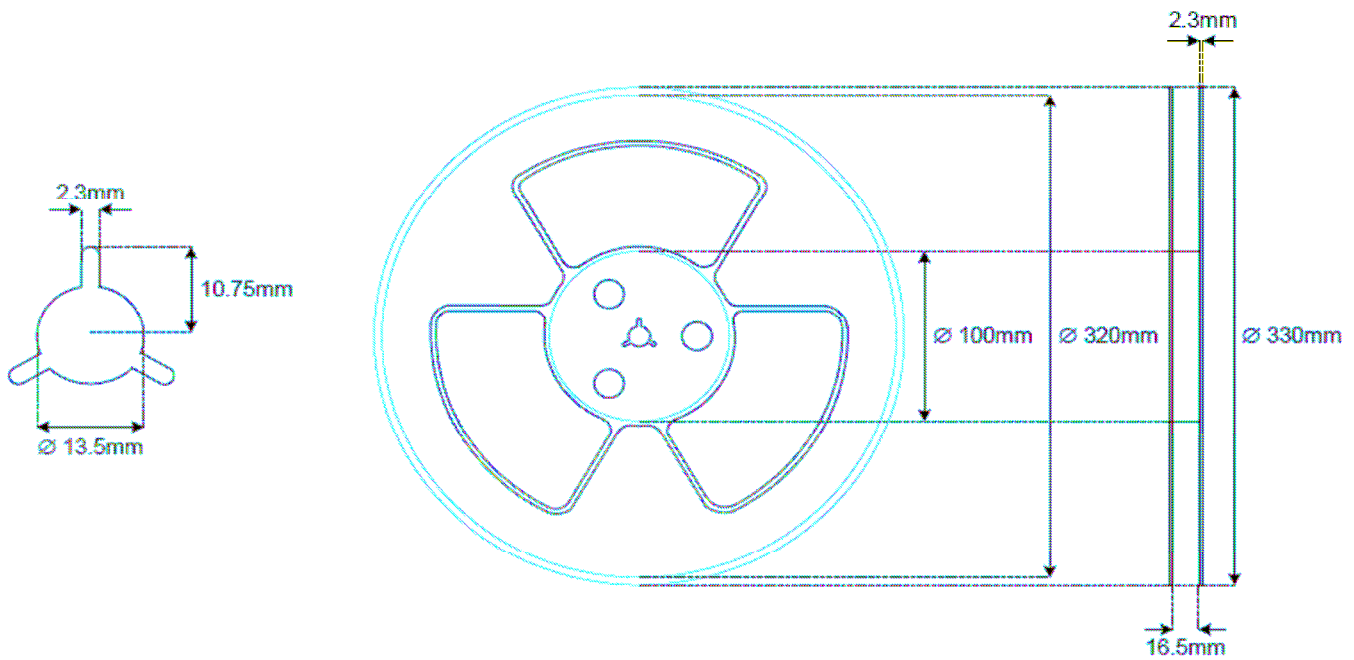


Figure 9. Dimensions of the reel

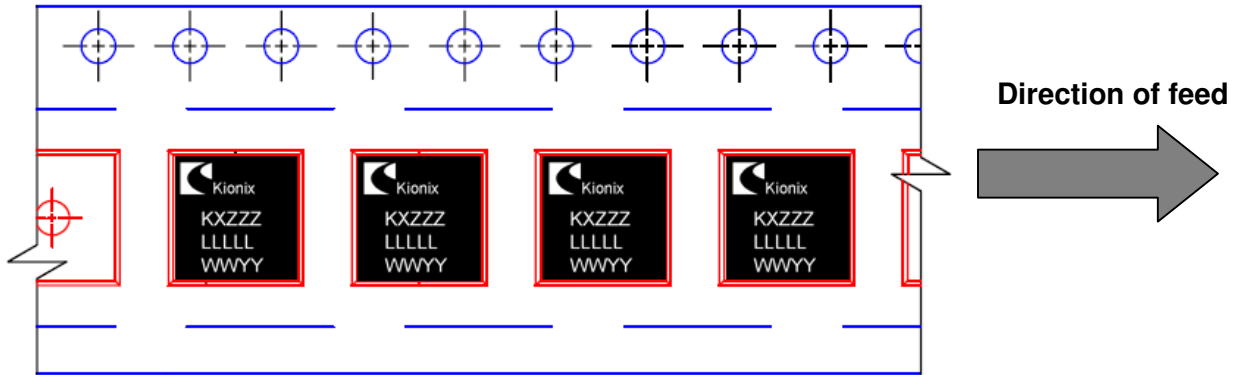


Figure 10. Orientation of the parts in the carrier tape and direction of feed

Revision History

Rev	Date	Description of Change
-	09-Oct-08	Initial release

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